WHAT IS CLAIMED IS:

1. A differential data transmitter comprising:

a first pre-driver configured to receive a differential data signal;

a delay circuit configured to receive the differential data signal in parallel with the first pre-driver, and output the differential data signal with a delay time, the delay circuit variably setting the delay time in accordance with a control signal;

a second pre-driver configured to receive an output signal from the delay circuit; and

an output driver configured to receive first and second output signals from the first and second pre-drivers, and output a pre-emphasis waveform signal that corresponds to a subtraction signal between the first and second output signals.

2. The transmitter according to claim 1, wherein the delay circuit comprises

first and second sub delay circuits configured to receive the differential data signal in parallel with each other, the first and second sub delay circuits providing signal delays different from each other, and

a delay output circuit configured to receive first and second sub output signals from the first and second sub delay circuits, and selectively use the first and second sub output signals to set the delay time.

3. The transmitter according to claim 2, wherein

the delay output circuit selectively outputs one of the first and second sub output signals.

4. The transmitter according to claim 2, wherein the delay output circuit mixes and outputs the first and second sub output signals at a certain ratio.

5. The transmitter according to claim 2, wherein each of the first and second sub delay circuits comprises a differential circuit including two MOS transistors, the two MOS transistors respectively have gates to be respectively supplied with positive and negative signals of the differential data signal, the two MOS transistors share a source connection node to which a constant current circuit is connected, and the two MOS transistors have drains to which load circuits are respectively connected.

6. The transmitter according to claim 2, wherein the delay output circuit comprises first and second differential circuits connected to an output thereof, in parallel with each other,

the first differential circuit comprises first and second MOS transistors, the first and second MOS transistors respectively have gates to be respectively supplied with positive and negative signals of the first sub output signal, the first and second MOS transistors share a source connection node to which a first current circuit is connected, and the first and second MOS transistors have drains to which load

circuits are respectively connected, and

the second differential circuit comprises third and fourth MOS transistors, the third and fourth MOS transistors respectively have gates to be respectively supplied with positive and negative signals of the second sub output signal, the third and fourth MOS transistors share a source connection node to which a second current circuit is connected, and the third and fourth MOS transistors have drains to which the load circuits are respectively connected.

7. The transmitter according to claim 6, wherein a current value is controllable in accordance with the control signal in one or both of the first and second current circuits.

8. The transmitter according to claim 1, further comprising another delay circuit connected to the delay circuit in series and configured to provide an input signal with a fixed delay time.

9. The transmitter according to claim 1, wherein the differential signal is a serial differential signal.

10. The transmitter according to claim 9, further comprises a parallel-serial converter configured to receive a parallel differential signal and output the serial differential signal.

11. A differential data transmitter-receiver apparatus comprising:

a transmitter configured to transmit a first data signal to an opposite-party differential data transmitter-receiver apparatus;

a receiver configured to receive a second data signal from the opposite-party differential data transmitter-receiver apparatus; and

a control section configured to control the transmitter and the receiver,

the transmitter comprising

a first pre-driver configured to receive a differential data signal,

a delay circuit configured to receive the differential data signal in parallel with the first pre-driver, and output the differential data signal with a delay time, the delay circuit variably setting the delay time in accordance with a control signal supplied from the control section,

a second pre-driver configured to receive an output signal from the delay circuit, and

an output driver configured to receive first and second output signals from the first and second pre-drivers, and output a pre-emphasis waveform signal that corresponds to a subtraction signal between the first and second output signals,

wherein the control section controls the delay circuit, based on a result of monitoring an eye pattern of the second data signal received by the receiver.

12. The transmitter-receiver apparatus according to claim 11, wherein the second data signal is derived from the first data signal, which has been received by the opposite-party differential data transmitter-receiver apparatus and returned to the receiver.

13. The transmitter-receiver apparatus according to claim 11, wherein each of the differential signal and the first and second data signal is a serial differential signal.

14. The transmitter-receiver apparatus according to claim 13, wherein the transmitter and the receiver respectively comprise a parallel-serial converter and a serial-parallel converter.

15. The transmitter-receiver apparatus according to claim 11, wherein the delay circuit comprises

first and second sub delay circuits configured to receive the differential data signal in parallel with each other, the first and second sub delay circuits providing signal delays different from each other, and

a delay output circuit configured to receive first and second sub output signals from the first and second sub delay circuits, and selectively use the first and second sub output signals to set the delay time.

16. The transmitter-receiver apparatus according to claim 15, wherein the delay output circuit selectively outputs one of the first and second sub output signals.

17. The transmitter-receiver apparatus according to claim 15, wherein the delay output circuit mixes and outputs the first and second sub output signals at a certain ratio.

18. The transmitter-receiver apparatus according to claim 11, further comprising another delay circuit connected to the delay circuit in series and configured to provide an input signal with a fixed delay time.